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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,010	12/13/2001	Scott Derner	400.119US01	2780

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,010	DERNER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 9-14 and 24-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 9-14 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over McConnell; Roderick et al. (US 5986952 A, hereafter referred to as McConnell) in view of Barth, Jr.; John E. et al. (US 5134616 A, hereafter referred to as Barth).

35 U.S.C. 103(a) rejection of claims 9 and 24.

McConnell teaches a method of operating a ROM embedded DRAM (col. 2, lines 40-67 and col. 1, lines 60-67 in McConnell teach that a DROM is a memory device with a ROM section built out of DRAM cells and embedded in DRAM so that some of the DRAM cells still function as DRAM, hence DROM is ROM embedded DRAM; Note: in Figure 1 of McConnell memory cells 11 and 13 are ROM cells and memory cells 12 are DRAM cells), comprising: receiving a row and column address to read data from a ROM section (Figure 1 of McConnell teaches the use of bit line addresses BADR and word line addresses WADR for accessing memory during read/write operations; Note: a bit line address BADR is a row address and a word line address WADR is a column address; Note also that claim 3 in McConnell teaches that memory is addressable and accessible for reading out data in units and that col.1, lines 16-28 in McConnell teach that units can be word or bit lines; Note: if the units are bit lines, then both the bit line row address BADR and the word line column address WADR are required to access data during read out since data is read out of bit lines, hence McConnell teaches receiving a bit line row addresses BADR and word line column addresses WADR to read data from a ROM unit); reading an encoded ROM bit using an error correcting code decoder (col. 4, lines 32-40 in McConnell teach that the E3 units are used to store parity data for the E1 units, hence the ROM units are encoded; col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for decoding the read ROM bit; Note: error correcting circuitry repair device 5 is used to read); and

correcting the read ROM bit if necessary (col. 4, lines 62-67 in McConnell teach the use of error correction codes for performing error correction).

However McConnell does not explicitly teach the specific use of presenting the corrected ROM bit as output data.

The Examiner asserts that memory is useless unless connected to other electronic devices needing storage. It is also obvious that corrected data would be provided to an application hardware device since correct data is necessary for correct system operation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of McConnell by including use of presenting the corrected ROM bit as output data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of presenting the corrected ROM bit as output data would have provided the opportunity to maintain correct system operation.

However McConnell does not explicitly teach the specific use of on-chip error correcting circuitry.

Barth, in an analogous art, teaches use of on-chip error correcting circuitry (see abstract in Barth).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McConnell with the teachings of Barth by including use of on-chip error correcting circuitry. This modification would have been obvious to one of

ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of on-chip error correcting circuitry would have provided reduced access delays (see abstract in Barth).

35 U.S.C. 103(a) rejection of claim 10.

McConnell teaches decoding the read ROM bit with error correcting circuitry (col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for decoding the read ROM bit); comparing the decoded ROM bit with the actual ROM bit (Note: error correction is a means for comparing decoded bits with actual ROM bits by comparing the read parity from the E3 units with the newly generated parity during decoding); and correcting if the decoded ROM bit differs from the read ROM bit (col. 4, lines 62-67 in McConnell teach that the error correction codes are used for performing error correction).

35 U.S.C. 103(a) rejection of claim 11.

Col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for error correcting.

35 U.S.C. 103(a) rejection of claim 12.

McConnell teaches generating an ECC corrected ROM bit from a read ROM bit (col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes); comparing the ECC corrected bit with the read ROM bit (col. 3, lines 22-25 in McConnell teach that read out data is compared with actual written data; Note: error correction is used in the read process, hence read data is error corrected data); and correcting the read ROM bit if the ECC corrected ROM bit and the read ROM bit do not match (col. 3, lines 22-28 in McConnell teach that the ROM bit is corrected by matching the address to a replacement E2 unit).

35 U.S.C. 103(a) rejection of claim 13.

McConnell teaches error correcting with parity checking (col. 3, lines 10-13 in McConnell).

35 U.S.C. 103(a) rejection of claim 14.

McConnell teaches comparing the parity check bit with the read ROM bit (Note: error correction is a means for comparing decoded bits with actual ROM bits by comparing the read parity ROM bits from the E3 units with the newly generated parity during decoding); and inverting the read ROM bit if the parity bit indicates an error (col. 4, lines 62-67 in McConnell teach that the error correction codes are used for performing error correction).

35 U.S.C. 103(a) rejection of claim 25.

McConnell and Barth substantially teaches the claimed invention described in claim 24 (as rejected above). In addition, McConnell teaches reading a unit of ROM data (Note that claim 3 in McConnell teaches that memory is addressable and accessible for reading out data in units and that col.1, lines 16-28 in McConnell teach that units can be word or bit lines); decoding the unit of ROM data (col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for decoding the read ROM unit); and determining if the ROM data is correct (Note: error correction is a means for comparing decoded bits with actual ROM bits by comparing the read parity from the E3 units with the newly generated parity during decoding to determine of the data is correct). However McConnell and Barth does not explicitly teach the specific use of a byte size unit.

The Examiner asserts that col.1, lines 16-28 in McConnell teach that units can be word or bit lines as an example but explicitly leaves the size of a unit open so that embodiment using any other unit size is an obvious engineering design choice. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to with the teachings of McConnell and Barth by including use of a byte size unit. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a byte size unit would have provided the opportunity to implement a particular embodiment of the McConnell based on obvious engineering design choices such as memory width bus width, error correction code, etc.

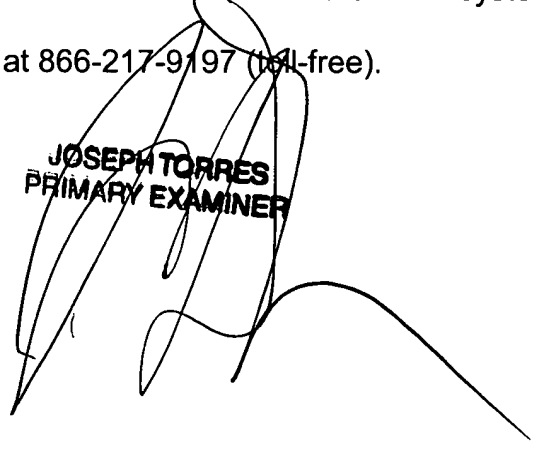
35 U.S.C. 103(a) rejection of claim 26.

McConnell teaches error correcting with parity checking (col. 3, lines 10-13 in McConnell).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133